

IN THE CLAIMS:

Claims 1-14 (Cancelled)

Claim 15 (Original) A semiconductor structure comprising

a semiconductor substrate having at least one trench isolation region located therein, said at least one trench isolation region having sidewalls that extend to a common bottom wall; and

a nitride liner present at least on portions of the sidewalls, said nitride liner protecting the sidewalls of the at least one trench so as to reduce stress in the semiconductor substrate.

Claim 16 (Original) The semiconductor structure of Claim 15 wherein the nitride liner is present on the entire sidewalls and bottom wall of the at least one trench.

Claim 17 (Original) The semiconductor structure of Claim 15 wherein the nitride liner is a nitrified surface layer that has a thickness of about 0.1 to about 2.0 nm.

Claim 18 (Original) The semiconductor structure of Claim 15 further comprising NFET device regions and PFET device regions.

Claim 19 (Original) The semiconductor structure of Claim 18 wherein the trenches adjoining the NFETs contain the nitride liner on the entire sidewalls and bottom wall of each trench.

Claim 20 (Original) The semiconductor structure of Claim 18 wherein the sidewalls of the trenches adjoining the PFETs are void of any nitride liner.